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4. ORIGINATOR		Defense Elec	Street, City, State, Zipetronics Supply Center		5. CAGE CODE 67268	6. NOR NO. 5962-R160-96		
a. TYPED NAME (Fir Last)	st, Middle Initial,	1507 Wilming Dayton, OH 4			7. CAGE CODE 67268	8. DOCUMENT NO. <b>86020</b>		
9. TITLE OF DOCUM	IENT			10. REVISION LETTI	FR	11. ECP NO.		
MICROCIRCUIT, 2 MONOLITHIC SILIO	56-BIT LOW POWER CON	SCHOTTKY BIF	POLAR RAM,	a. CURRENT A	b. NEW B	N/A		
12. CONFIGURATIO All	N ITEM (OR SYSTEM	I) TO WHICH EC	P APPLIES	,				
13. DESCRIPTION C	F REVISION							
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	(2) Revised docum	ent must be recei	ived before manufactu	rer may incorporate this	change.			
	(3) Custodian of ma	aster document s	ived before manufactu					
c. TYPED NAME (First, Middle Initial, Last)								
DESC-ELDS Michael A. Frye								
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Defense Electronics			PREPARED BY Rick C. Officer					MILITARY DRAWING  This drawing is available for use by all Departments and							and					
Supply Center Dayton, Ohio	er	•	,		CKED Di Ce						Agend	cies o	of the I	Depar	tment	of De	fense			
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# 1. SCOPE

- 1.1 Scope. This drawing describes device requirements for class B microcircuits in accordance with 1.2.1 of MIL-STD-883 "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices".
  - 1.2 Part number. The complete part number shall be as shown in the following example:



1.2.1 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number	<u>Circuit</u>	Access time
01	27LS00	256-bit low power Schottky bipolar	55 ns
		RAM three-state	
02	27LS00A	256-bit low power Schottky bipolar	45 ns
		RAM three-state	
03	27LS01	256-bit low power Schottky bipolar	55 ns
		RAM open collector	
04	27LS01A	256-bit low power Schottky bipolar	45 ns
		RAM open collector	

1.2.2 <u>Case outlines</u>. The case outlines shall be as designated in appendix C of MIL-M-38510, and as follows:

Outline letter	Case outline
E	D-2 (16-lead, 1/4" x 7/8"), dual-in-line package
F	F-5 (16-lead, 1/4" x 3/8"), flat package

#### 1.3 Absolute maximum ratings.

Supply voltage range .....-0.5 V dc to +7.0 V dc Input voltage range .....-0.5 V dc to +5.5 V dc Storage temperature range  $~\dots \dots -65^{\circ}\text{C}$  to +150°C

Thermal resistance, junction-to-case ( $\theta_{JC}$ ):

Case E ...... (See MIL-M-38510, appendix C) Case F ...... (See MIL-M-38510, appendix C)

Junction temperature (T<sub>J</sub>) .....+175°C 

DC input current .....-30 mA to +5 mA

## 1.4 Recommended operating conditions.

Maximum low-level input voltage  $(V_{IL})^{''}$  . . . . . . . 0.8 V dc Case operating temperature range  $(T_C)$  . . . . . -55°C to +125°C

 $\underline{1}/$  Must withstand the added PD due to short circuit test (e.g., IOS).

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#### 2. APPLICABLE DOCUMENTS

2.1 <u>Government specification and standard</u>. Unless otherwise specified, the following specification and standard, of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

## **SPECIFICATION**

**MILITARY** 

MIL-M-38510 - Microcircuits, General Specification for.

**STANDARD** 

**MILITARY** 

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Copies of the specification and standard required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

#### 3. REQUIREMENTS

- 3.1 <u>Item requirements</u>. The individual item requirements shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified ir MIL-M-38510 and herein.
  - 3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.
  - 3.2.2 Truth table. The truth table shall be as specified on figure 2.
  - 3.2.3 Logic diagrams. The logic diagrams shall be as specified on figure 3.
  - 3.2.4 <u>Case outlines</u>. The case outlines shall be in accordance with 1.2.2.
- 3.3 <u>Electrical performance characteristics</u>. Unless otherwise specified, the electrical performance characteristics are as specified in table I and apply over the full recommended case operating temperature range.
- 3.4 <u>Marking</u>. Marking shall be in accordance with MIL-STD-883 (see 3.1 herein). The part shall be marked with the part numbe listed in 1.2 herein. In addition, the manufacturer's part number may also be marked as listed in 6.4 herein.
- 3.5 <u>Certificate of compliance</u>. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in 6.4. The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply shal state that the manufacturer's product meets the requirements of MIL-STD-883 (see 3.1 herein) and the requirements herein.
- 3.6 <u>Certificate of conformance</u>. A certificate of conformance as required in MIL-STD-883 (see 3.1 herein) shall be provided with each lot of microcircuits delivered to this drawing.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions	Group A	Device	Limits		Unit
Test	Зупьог	-55° C ≤ T <sub>C</sub> ≤ +125° C 4.5 V ≤ V <sub>CC</sub> ≤ 5.5 V	subgroups	type	Min	Max	
Output high voltage	V <sub>OH</sub>	$V_{CC}$ = minimum $I_{OH}$ = -2.0 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$	1, 2, 3	01, 02	2.4		V
Output low voltage	V <sub>OL</sub>	$V_{CC}$ = minimum $I_{OL}$ = 16 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$	1, 2, 3	All		0.45	V
Input high level	V <sub>IH</sub>	Guaranteed input logical high voltage for all inputs 1/	1, 2, 3	All	2.0		V
Input low level	V <sub>IL</sub>	Guaranteed input logical low voltage for all inputs 1/	1, 2, 3	All		0.8	V
Input low current	I <sub>IL</sub>	V <sub>CC</sub> = maximumV <sub>IN</sub> = 0.4 V	1, 2, 3	All		-0.25	mA
Input high current	I <sub>IH</sub>	V <sub>CC</sub> = maximumV <sub>IN</sub> = 2.7 V	1, 2, 3	All		20	μА
Output short circuit current	los	V <sub>CC</sub> = maximum V <sub>OUT</sub> = 0.0 V	1, 2, 3	01, 02	-20	-60	mA
Power supply current	lcc	All inputs = GND V <sub>CC</sub> = Maximum	1, 2, 3	02, 04 01, 03		115 70	mA
Input clamp voltage	V <sub>CL</sub>	V <sub>CC</sub> = Minimum, I <sub>IN</sub> = -18 mA	1, 2, 3	All		-1.2	V
Output leakage current	I <sub>CEX</sub>	$V_{CS} = V_{IH} \text{ or } V_{WE} = V_{IL}$ $V_{OUT} = 2.4 \text{ V}$	1, 2, 3	All		30	μА
		$V_{CS} = V_{IH} \text{ or } V_{WE} = V_{IL}$ $V_{OUT} = 0.4 \text{ VV}_{CC} = \text{maximum}$	1, 2, 3	01, 02	-30		μА

See footnote at end of table.

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 $\label{eq:table_performance} \mbox{TABLE I. } \underline{\mbox{Electrical performance characteristics}} \mbox{ - Continued.}$ 

Test	Symbol	Conditions $-55^{\circ} \text{ C} \leq \text{T}_{\text{C}} \leq +125^{\circ} \text{ C}$ $4.5 \text{ V} \leq \text{V}_{\text{CC}} \leq 5.5 \text{ V}$	Group A	Device	Limits	Unit	
1631	Cymbol		subgroups	type	Min	Max	
Delay from address	t <sub>PLH</sub> (A) t <sub>PHL</sub> (A)	See figure 4 2/3/4/	9, 10, 11	01, 03		55	ns
to output	t <sub>PHL</sub> (A)			02, 04		45	
Delay from chip select (low) to	t <sub>PZH</sub> (CS)		9, 10, 11	01, 03		30	ns
active output and correct data	t <sub>PZL</sub> (CS) <u>5</u> /			02, 04		25	
Delay from write	t <sub>PZH</sub> (WE)	See figures 4, 5, and 6	9, 10, 11	01, 03		55	ns
enable (high) to	5/ _	<u>2/3/4/</u>	3, 10, 11	02, 04		45	
active output	t <sub>PZL</sub> (WE)			01, 03		55	I
and correct data	<u>5</u> /			02, 04		45	
Setup time address (prior to initiation of write)	t <sub>S</sub> (A)		9, 10, 11	All	5		ns
Hold time address (after termina- tion of write)	t <sub>h</sub> (A)		9, 10, 11	All	5		ns
Setup time data input (prior to	t <sub>s</sub> (DI)		9, 10, 11	01, 03	35		ns
termination of write)				02, 04	30		ns
Hold time data input (after termination of write)	t <sub>h</sub> (DI)		9, 10, 11	All	5		ns
Minimum write enable pulse width to insure	t <sub>pw</sub> (WE)		9, 10, 11	01, 03	35		ns
write				02, 04	30		ns

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions	Group A	Device	Limits		Unit
	Cysc.	$-55^{\circ}$ C $\leq$ T <sub>C</sub> $\leq$ +125° C 4.5 V $\leq$ V <sub>CC</sub> $\leq$ 5.5 V	subgroups	type	Min	Max	_
Delay from chip select (high) to	t <sub>PHZ</sub> (CS)	See figure 4 2/3/4/	9, 10, 11	01, 03		30	ns
inactive output (HI-Z)	t <sub>PLZ</sub> (CS)			02, 04		25	ns
Delay from write enable (low) to	t <sub>PLZ</sub> (WE)		9, 10, 11	All		40	ns
inactive output (HI-Z)	$t_{PHZ}(WE)$						

- 1/ These are absolute voltages with respect to device ground pin and include all overshoots due to system or tester noise, or both. Do not attempt to test these values without suitable equipment.
- 2/ Output is preconditioned to data in during write to ensure correct data is present on all outputs when write is terminated. (No write recovery glitch).
- 3/ t<sub>PLH</sub>(A) and t<sub>PHL</sub>(A) are tested with S closed and C<sub>L</sub> = 50 pF with both input and output timing referenced to 1.5 V.
- For open collector (03, 04), all delays from write enable (WE) or chip select (CS) inputs to the data output (D<sub>OUT</sub>),  $t_{PLZ}(WE)$ ,  $t_{PLZ}(CS)$ ,  $t_{PLZ}(WE)$ , and  $t_{PZL}(CS)$  are measured with S closed and  $C_L = 50$  pF and with both the input and output timing referenced to 1.5 V.
- For three-state output (01, 02)  $t_{PZH}(WE)$  and  $t_{PZH}(CS)$  are <u>me</u>asure<u>d</u> with <u>S</u> open,  $C_L = 50$  pF and with both the input and output timing referenced to 1.5 V.  $t_{PZL}(WE)$  and  $t_{PZL}(CS)$  are measured with <u>S</u> \_\_ closed,  $C_L = 50$  pF and with both the input and output timing referenced to 1.5 V.  $t_{PHZ}(WE)$  and  $t_{PHZ}(CS)$  are measured with <u>S</u> open and  $C_L < 5$  pF and are measured between the 1.5 V level on the input to the  $V_{OH}$  -500 mV level on the output.  $t_{PLZ}(WE)$  and  $t_{PLZ}(CS)$  are measured with <u>S</u> closed and  $C_L < 5$  pF and are measured between the 1.5 V level on the input and the  $V_{OL} + 500$  mV level on the output.

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- 3.7 <u>Notification of change</u>. Notification of change to DESC-ECS shall be required in accordance with MIL-STD-883 (see 3.1 herein).
- 3.8 <u>Verification and review</u>. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

## 4. QUALITY ASSURANCE PROVISIONS

- 4.1 <u>Sampling and inspection</u>. Sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein).
- 4.2 <u>Screening</u>. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:
  - a. Burn-in test (method 1015 of MIL-STD-883).
    - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
    - (2)  $T_A = +125^{\circ} C$ , minimum.
  - b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.
- 4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.
  - 4.3.1 Group A inspection.
    - a. Tests shall be as specified in table II herein.
    - b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.
    - c. Subgroup 4 (C<sub>IN</sub> measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.
  - 4.3.2 Groups C and D inspections.
    - a. End-point electrical parameters shall be as specified in table II herein.
    - b. Steady-state life test (method 1005 of MIL-STD-883) conditions:
      - (1) Test condition A, B, C, or D using the circuit submitted with the certificate of compliance (see 3.5 herein).
      - (2)  $T_{\Delta} = +125^{\circ} \text{ C}$ , minimum.
      - (3) Test duration: 1,000 hours, except as permitted by appendix B of MIL-M-38510 and method 1005 of MIL-STD-883.

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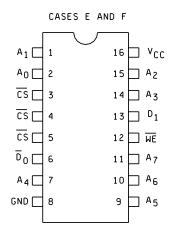


FIGURE 1. Terminal connections.

	Input		Data output	Mode
CS	WE	D1	Status DO (t <sub>n</sub> + 1)	
Н	Х	Х	Output disabled	No selection
L	L	L	Output disabled	Write '0'
L	L	Н	Output disabled	Write '1'
L	Н	Х	Selected bit (inverted)	Read

H = High L = Low

X = Don't care

FIGURE 2. Truth table.

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# DEVICE TYPES 01 AND 02

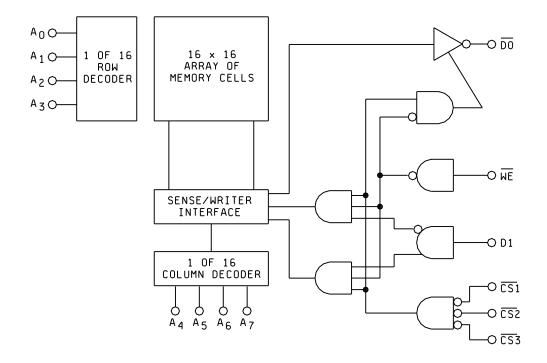


FIGURE 3. Logic diagrams.

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# DEVICE TYPES 03 AND 04

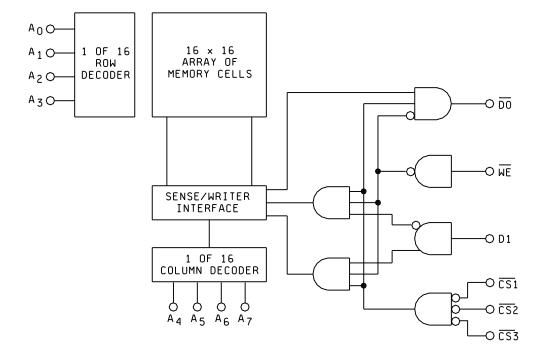


FIGURE 3. Logic diagrams - Continued.

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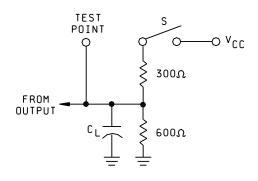


FIGURE 4. Switching test circuit.

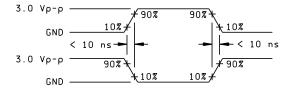


FIGURE 5. Switching test waveform.

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# 

t<sub>PZL</sub>(WE)MAX

t<sub>PZH</sub>(WE)MAX

WRITE MODE

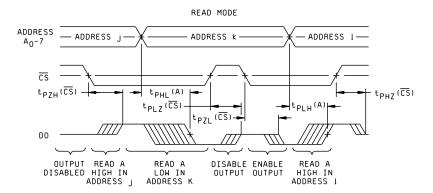
Write Cycle Timing. The cycle is initiated by an address change. After  $t_{\rm S}(A)$  max, the write enable may begin. The chip select must also be LOW for writing. Following the write pulse,  $t_{\rm h}(A)$  max must be allowed before the address may be changed again. The output will be inactive (floating for device types 01 and 02) while the write enable is LOW. Ordinarily, the chip select should be LOW during the entire write pulse.

t<sub>PLZ</sub>(WE)MAX -

FIGURE 6. Switching waveforms.

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DO I<sub>F</sub>CS=L



Switching delays from address and chip select inputs to the data output. For devices 01 and 02, disabled output is "OFF", represented by a single center line. For devices 03 and 04 a disabled output is HIGH.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUT	ОИТРИТ
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

FIGURE 6. Switching waveforms - Continued.

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TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (per method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7, 8, 9, 10, 11**
Group A test requirements (method 5005)	1, 2, 3, 7, 8, 9, 10, 11**
Groups C and D end-point electrical parameters (method 5005)	1, 2, 3
Additional electrical subgroups for group C periodic inspections	

<sup>\*</sup> PDA applies to subgroup 1.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510.

#### 6. NOTES

- 6.1 <u>Intended use.</u> Microcircuits conforming to this drawing are intended for use when military specifications do not exist and qualified military devices that will perform the required function are not available for OEM application. When a military specification exists and the product covered by this drawing has been qualified for listing on QPL-38510, the device specified herein will be inactivated and will not be used for new design. The QPL-38510 product shall be the preferred item for all applications.
- 6.2 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.
- 6.3 <u>Comments</u>. Comments on this drawing should be directed to DESC-ECS, Dayton, Ohio 45444, or telephone 513-296-5375.

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<sup>\*\*</sup> Subgroups 10 and 11, if not tested, shall be guaranteed to the specified limits in table I. Subgroups 7 and 8 shall consist of verifying the truth table specified on figure 2.

6.4 <u>Approved source of supply</u>. An approved source of supply is listed herein. Additional sources will be added as they become available. The vendor listed herein has agreed to this drawing and a certificate of compliance (see 3.5 herein) has been submitted to DESC-ECS.

Military drawing part number	Vendor	Vendor	Replacement
	CAGE	similar part	military specification
	number	number <u>1</u> /	part number
8602001EX 8602001FX 8602002EX 8602002FX 8602003EX 8602003FX 8602004EX 8602004FX	34335 34335 34335 34335 34335 34335 2/ 2/	AM27LS00/BEA AM27LS00/BFA AM27LS00A/BEA AM27LS00A/BFA AM27LS01/BEA AM27LS01/BFA AM27LS01A/BEA AM27LS01A/BEA	    

- 1/ Caution: Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 2/ Not available from an approved source of supply.

34335

 Vendor CAGE
 Vendor name

 number
 and address

Advanced Micro Devices, Incorporated 901 Thompson Place P. O. Box 3453 Sunnyvale, CA 94088

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